WHAT IS CLAIMED IS:

1. A method for processing a semiconductor topography comprising diffusing deuterium across one or more layer interfaces of a silicon-oxide-nitride-oxide-silicon structure during a reflow of a dielectric layer spaced above the silicon-oxide-nitride-oxide-silicon structure.

2. The method of claim 1, wherein said diffusing deuterium across the one or more layer interfaces comprises introducing deuterium into at least one of the one or more layer interfaces.

3. The method of claim 1, wherein said diffusing comprises diffusing deuterium across an interface between a lower silicon layer and a lower oxide layer of the silicon-oxide-nitride-oxide-silicon structure.

4. The method of claim 1, wherein said diffusing comprises diffusing deuterium across an interface between an upper silicon layer and an upper oxide layer of the silicon-oxide-nitride-oxide-silicon structure.

5. The method of claim1, wherein said silicon-oxide-nitride-oxide-silicon structure comprises a deutereated nitride layer prior to said reflow.

6. The method of claim 1, further comprising:

forming a deutereated nitride layer above the silicon-oxide-nitride-oxide-silicon structure; and

depositing the dielectric layer above the deutereated nitride layer prior to said reflow.

7. The method of claim 6, wherein said depositing the dielectric layer comprises depositing a deutereated dielectric layer.

8. The method of claim 6, further comprising annealing the semiconductor topography prior to said forming the deutereated nitride layer, wherein said annealing comprises introducing deuterium into the semiconductor topography.

9. A method for processing a semiconductor topography, comprising:

annealing the semiconductor topography with a deutereated substance; and

forming a deutereated nitride layer above the semiconductor topography subsequent to said annealing.

10. The method of claim 9, wherein said annealing comprises introducing deuterium into an upper portion of the semiconductor topography.

11. The method of claim 9, wherein said annealing comprises exposing the semiconductor topography to deutereated ammonia.

12. The method of claim 9, wherein said forming the deutereated nitride layer comprises forming the deutereated nitride layer above a silicon-oxide-nitride-oxide-silicon structure arranged within the semiconductor topography.

13. The method of claim 12, further comprising:

depositing a dielectric layer above the deutereated nitride layer; and

reflowing the dielectric layer, wherein said reflowing comprises diffusing deuterium across one or more interfaces of the silicon-oxide-nitride-oxide-silicon structure.

14. The method of claim 13, wherein said reflow comprises exposing the semiconductor topography to an ambient comprising a deutereated substance.

15. The method of claim 9, wherein said forming the deutereated nitride layer comprises forming the deutereated nitride layer upon and in contact with an oxide-silicon bilayer stack arranged within the semiconductor topography.

16. The method of claim 15, further comprising depositing a second oxide-silicon bilayer stack upon the nitride layer to form a silicon-oxide-nitride-oxide-silicon structure.

17. A silicon-oxide-nitride-oxide-silicon structure, comprising:

a first silicon layer comprising an undoped lower portion; and

a first oxide layer arranged upon the first silicon layer, wherein an interface between the first silicon layer and the first oxide layer comprises deuterium.

18. The silicon-oxide-nitride-oxide-silicon structure of claim 17, wherein a lateral length of the interface between the first silicon layer and the first oxide layer is bound by opposing sidewalls of the structure, and wherein said deuterium is arranged across an entirety of said lateral length.

19. The silicon-oxide-nitride-oxide-silicon structure of claim 17, further comprising:

a nitride layer arranged upon and in contact with the first oxide layer;

a second oxide layer arranged upon and in contact with the nitride layer; and

a second silicon layer arranged upon and in contact with the second oxide layer, wherein an interface between the second silicon layer and second oxide layer comprises deuterium.

20. The silicon-oxide-nitride-oxide-silicon structure of claim 19, wherein said nitride layer comprises deuterium.